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(54) Memory device

(57) A memory device includes a standard memory core, an input buffer receiving an external clock signal and producing an internal clock signal, an output path of data read from the standard memory core comprising a state machine receiving the internal clock signal for controlling the data stream coupled to the output of the standard memory through a first internal data bus, and an output buffer coupled to the output of the state machine through a second internal bus and comprising an output stage enabled by the state machine for producing the read data on an output bus.

The memory device of the invention outputs the read data in a time starting from the rising edge of the external clock that is shorter than that of other known devices, because the output buffer has an array of master-slave pairs of flip-flops synchronized by respective timing signals derived from the internal clock signal, said array receiving data from the state machine through the second internal bus and providing the data to be output to the output stage of the buffer enabled by the state machine. A logic circuit generates timing signals for the master-slaves flip-flops, respectively as logic NAND and logic AND of the internal clock signal and of an enabling signal of the output stage of the buffer generated by the state machine. Moreover, the memory device comprises a circuit, synchronized by the internal clock signal, that introduces a delay of the enabling signal of the output stage of the buffer equivalent to a period of the internal clock signal.

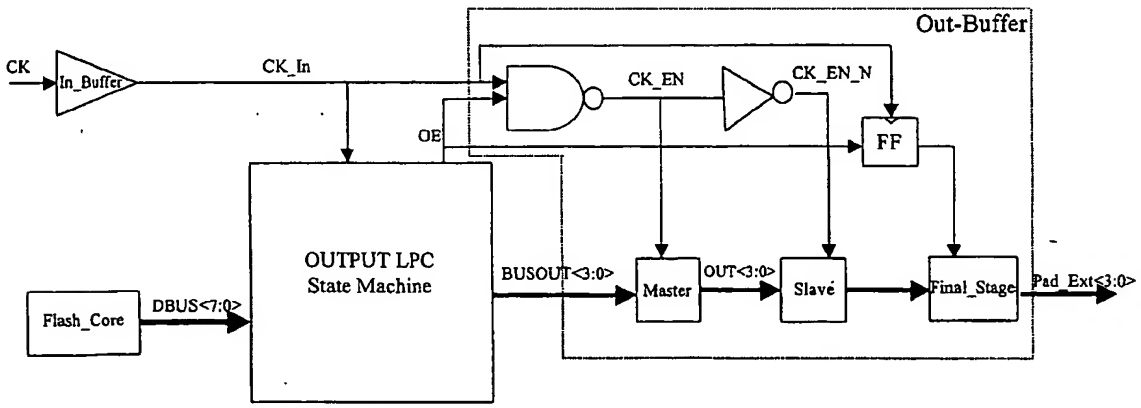

Fig. 5

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Description

FIELD OF THE INVENTION

[0001] The present invention relates in general to memory devices and in particular to a memory device with a reduced output time of a datum read from the memory.

BACKGROUND OF THE INVENTION

[0002] There are many applications for volatile and non volatile memory devices, such as digital cameras, measurement instruments and the like.

[0003] A functional block diagram of a common memory device is shown in Figure 1, purposely emphasizing only the output path of a datum read from the memory. The data output path includes essentially a state machine OUTPUT_LPC controlling the stream of data as they are read from a standard memory core FLASH_CORE and placed on a first internal data bus DBUS<7:0> and an output buffer OUT_BUFFER, coupled to the state machine through a second internal bus BUSOUT<3:0>.

[0004] An internal timing signal CK_IN, generated by the internal buffer IN_BUFFER input with the external clock CK, synchronize the execution of the operations of the state machine. The state machine receives data coming from the standard memory core FLASH_CORE through the internal data bus DBUS<7:0>, which may typically be an eight bit bus, and conveys them in serial mode with a proper timing to the output buffer OUT_BUFFER. This buffer is enabled by an enabling signal OE generated by the state machine and is essentially constituted by an output stage FINAL_STAGE that produces the data on the output bus PAD_EXT<3:0>.

[0005] Several largely used protocols require that the datum read from the memory be made available on the output bus PAD_EXT<3:0> by a pre-established maximum time starting from the rising edge of the external clock.

[0006] Because of delays of propagation of digital signals through the circuitry present along the output path of the memory device, it may be difficult to meet such a fundamental specification.

[0007] In order to illustrate more clearly the addressed technical problem, a well known type of memory device will be considered in conjunction with an equally well known type of protocol that specifically sets such a maximum time.

[0008] In the ensuing description, reference will be made to a LPC (Low Pin Count) protocol, which is particularly important because of its popularity and widespread use, however all the considerations that will be made are valid *mutatis mutandis* even for other protocols setting the same requirement, such as the well known PCI and SPI protocols.

[0009] For each cycle of the LPC protocol, only one byte is read in the way illustrated in Figure 2. For the first 12 clock pulses, the external host of the memory device controls a system bus I/O (not shown in Figure 1) connected to the output bus PAD_EXT<3:0>. During this first group of clock pulses the external host provides codes to the input circuits of the memory device for accessing the standard memory core thereof FLASH_CORE.

[0010] The sequence of twelve clock pulses is so subdivided: one pulse for the START phase, one pulse for the CYCLE_TYPE phase that specifies whether the cycle of the LPC protocol is a READ or a WRITE cycle, eight clock pulses for the ADDRESS phase, in which the address of the memory sector in which the host must read or write data is provided, and two pulses for the TAR and TAR-Z phases signaling the handing over of the control on the system bus. After these last two clock cycles, the standard memory FLASH_CORE engages the system bus through the bus PAD_EXT<3:0>.

[0011] Let us suppose that the memory device has received through an input interface all information necessary to carry out a READ command, through the sequence exemplified in Figure 3.

[0012] After the TAR phase, within the memory FLASH_CORE an "Address Transition Detection" (ATD) signal is produced and thus a reading, asynchronous in respect of the external clock CK, is started.

[0013] The memory FLASH_CORE generates wait cycles, SYNC, during which it carries out internal operations. When the reading is completed, it outputs the read data and, by way of two further TAR cycles it transfers again the control of the system bus to the external host.

[0014] The state machine OUTPUT_LPC manages the transfer phase of the data read from the internal bus DBUS<7:0> to the output buffer OUT_BUFFER and, at the end of the process, it enables the output buffer to produce the read data on the output bus PAD_EXT<3:0>.

[0015] The internal clock signal CK_IN is input to the state machine that controls the data stream OUTPUT_LPC and the state machine generates a logic enable signal OE of the output buffer after two periods of the internal clock signal CK_IN, as required by the specifications of the LPC protocol, thus loading the data present on the first internal bus DBUS<7:0> on the second internal bus BUSOUT<3:0>.

[0016] As stated before, the LPC specifications, as the specifications of similar protocols, establish a maximum output time starting from the rising edge of the external clock CK for producing the read data on the output bus. Such a maximum time delay TVAL must be respected each time the memory must load data on the first internal bus DBUS<7:

0>.

[0017] As depicted in Figure 4, when two periods of the internal clock signal CK_IN have elapsed after that the datum to be read had been made available on the internal data bus DBUS<7:0>, the state machine OUTPUT_LPC generates the enabling signal OE and produces the datum to be read on the bus BUSOUT<3:0>.

[0018] After a certain delay TOUT_BUF, introduced by the output buffer OUT_BUFFER, the datum is finally produced on the output bus PAD_EXT<3:0>.

[0019] Because of propagation delays through the circuits of the output path, the datum to be read is made available on the bus PAD_EXT<3:0> after a time TVAL from the rising edge of the external clock CK. The time TVAL is the sum of three contributions:

- the delay TIO_BUF of the internal clock signal CK_IN in respect to the external clock signal CK;
- the load time TBUSOUT of data read from the memory on the second internal bus BUSOUT<3:0>,
- the delay introduced by the output buffer TOUT_BUF;

thus

$$TVAL = TIO\_BUF + TBUSOUT + TOUT\_BUF \quad (1)$$

[0020] Without an accurate design of the circuits of the output path of the memory device, the time TVAL may easily exceed the maximum delay in respect to the rising edge of the external clock CK allowed by the particular protocol being used.

OBJECT AND SUMMARY OF THE INVENTION

[0021] It has been found and is the object of the present invention a memory device capable of outputting data read from the memory with a maximum delay TVAL from the rising edge of an external clock signal sensibly shorter than the delay experienced in known devices manufactured with the same fabrication technology.

[0022] The gist of this invention consists in using master-slave pairs of flip-flops synchronized by respective timing signals and in loading in the output buffer the datum to be output after a single clock pulse.

[0023] More precisely the object of the invention is a memory device including a standard memory core, an input buffer receiving an external clock signal and producing an internal clock signal, an output path of data read from the standard memory core comprising a state machine receiving the internal clock signal for controlling the data stream coupled to the output of the standard memory through a first internal data bus, and an output buffer coupled to the output of the state machine through a second internal bus and comprising an output stage enabled by the state machine for producing the read data on an output bus.

[0024] The memory device of the invention outputs the read data in a time starting from the rising edge of the external clock that is shorter than that of other known devices, because the output buffer has an array of master-slave pairs of flip-flops synchronized by respective timing signals derived from the internal clock signal, said array receiving data from the state machine through the second internal bus and providing the data to be output to the output stage of the buffer enabled by the state machine. A logic circuit generates timing signals for the master-slaves flip-flops, respectively as logic NAND and logic AND of the internal clock signal and of an enabling signal of the output stage of the buffer generated by the state machine. Moreover, the memory device comprises a circuit, synchronized by the internal clock signal, that introduces a delay of the enabling signal of the output stage of the buffer equivalent to a period of the internal clock signal.

[0025] Preferably, the enabling logic signal of the output stage of the buffer is generated after a period of the internal clock signal starting from the instant in which the datum to be output is provided by the standard memory core to the state machine controlling the bit stream.

[0026] The delay circuit may be a D type flip-flop, that may be physically included either in the output buffer circuit block or in the state machine circuit block.

[0027] The invention is more precisely defined in the annexed claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The different aspects and advantages of the invention will become even more evident through a detailed description of an embodiment and by referring to the attached drawings, wherein:

Figure 1 is a basic diagram of a known memory device;

Figure 2 is a possible asynchronous sequence of cycles in managing a memory device;
Figure 3 compares the sequence of Figure 2 with the external clock signal of the memory device;
Figure 4 is a diagram of the main signals of the device of Figure 1;
Figure 5 is a basic diagram of a preferred embodiment of the memory device of the invention with an output buffer comprising an array of master and slave flip-flop pairs, a delay circuit and a logic circuit generating respective timing signals;
Figure 6 is a diagram of the main signals of the device of Figure 5.

DESCRIPTION OF AN EMBODIMENT OF THE INVENTION

[0029] The output path of data from a standard memory FLASH_CORE, according to a preferred embodiment of the memory device of the invention, is depicted in Figure 5. Differently from known devices, the device of the invention has an output buffer including an array of master and slave flip-flop pairs MASTER SLAVE, receiving respective timing signals CK_EN and CK_EN_N. The output buffer further comprises a logic circuit for generating the timing signals CK_EN and CK_EN_N and a delay circuit FF of the output stages enabling signal OE, by a period of the internal clock signal CK_IN.

[0030] As depicted in Figure 6, when the output enabling signal OE is active, the timing signals CK_EN and CK_EN_N switch, because they are generated as logic NAND and logic AND, respectively, of the internal clock signal CK_IN and of the output enabling signal OE. The data to be read are provided on the bus BUSOUT<3:0> of the state machine OUTPUT_LPC, and on the successive rising edge of the CK_EN signal, the array of flip-flops MASTER read them and inputs them to the array of flip-flops SLAVE through the bus OUT<3:0>.

[0031] The flip-flops SLAVE read the signal present at their input on the rising edge of the CK_EN_N signal or, alternatively, on the falling edge of the signal CK_EN, and transfer it to the output stage FINAL_STAGE. This stage outputs data on the output bus PAD_EXT<3:0> when the enabling signal OE is active.

[0032] Once the signal OE is activated, the signal CK_EN_N is a replica of the external clock CK delayed by a time TIO_BUF introduced by the input stage IN_BUFFER. The output stage FINAL_STAGE thus receives the datum to be placed on the output bus PAD_EXT<3:0> after a time TIO_BUF starting from the rising edge of the external clock CK.

[0033] Being TOUT_BUF the response time of the output stage FINAL_STAGE, data read from the memory are available on the output bus PAD_EXT<3:0> after a time TVAL from the rising edge of the external clock CK given by

$$TVAL = TIO\_BUF + TOUT\_BUF \quad (2)$$

which is smaller than that (1) of known memory devices. Therefore, the memory device of the invention is better suited than the prior art devices for protocols like the well known PCI and SPI protocols, which place a stringent limit on the maximum value of TVAL.

[0034] Preferably, for not delaying the production of data on the output bus PAD_EXT<3:0> from the instant they are placed on the internal bus DBUS<7:0>, the output enabling signal OE is activated after a single period of the internal clock signal CK_IN from the instant in which the datum to be output is provided to the state machine OUTPUT_LPC, as depicted in Figure 6. However, this feature is not essential for overcoming the considered technical problem.

[0035] It may be noticed that by generating the signal OE in advance by a clock period compared with what is done in known memory devices, does not contravene any specification of the considered protocol. In fact, the output stage FINAL_STAGE remains disabled for at least two periods of the internal clock signal from the instant in which the data to be output are provided to the state machine OUTPUT_LPC, as required by PCI protocols.

[0036] Preferably, the delay circuit FF is constituted by a D type flip-flop, synchronized by the internal clock signal CK_IN. The delay circuit may even be incorporated in the circuitry of the state machine OUTPUT_LPC controlling the data stream. That is the machine may provide on distinct output nodes the enabling signal OE and a replica thereof delayed by a period of the internal clock, respectively; for the logic circuit that generates the timing signals of the master/slave flip-flop and for the output stage.

[0037] The memory device according to the invention may include either a volatile or a non volatile standard memory core and may use a PCI bus and a Low Pin Count type state machine OUTPUT_LPC.

Claims

1. A memory device having a standard memory core (FLASH_CORE), an input buffer (IN_BUFFER) receiving an external clock signal (CK) and generating an internal clock signal (CK_IN), an output path for the data read from the memory core (FLASH_CORE) including a state machine (OUTPUT_LPC) receiving said internal clock signal

(CK_IN) for controlling the data stream coupled to the output of the memory core (FLASH_CORE) through a first internal data bus (DBUS<7:0>), and an output buffer (OUT_BUFFER) coupled to the output of the state machine (OUTPUT_LPC) through a second internal bus (BUSOUT<3:0>) and having an output stage (FINAL_STAGE) enabled by said state machine (OUTPUT_LPC) for producing on an output bus (PAD_EXT<3:0>) the read data, **characterized in that** said output buffer (OUT_BUFFER) comprises;

an array of master and slave pairs of flip-flops (MASTER, SLAVE) enabled by respective timing signals (CK_EN, CK_EN_N) derived from said internal clock signal (CK_IN), receiving data produced from said state machine (OUTPUT_LPC) on said second internal bus (BUSOUT<3:0>) and providing them to the output stage (FINAL_STAGE) for producing them on said output bus (PAD_EXT<3:0>);
a logic circuit generating said respective timing signals (CK_EN, CK_EN_N), respectively as the logic NAND and the logic AND of said internal clock signal (CK_IN) and of an enabling signal (OE) of the output stage (FINAL_STAGE) generated by said state machine (OUTPUT_LPC); and
a delay circuit (FF), synchronized by said internal clock signal (CK_IN), providing to an enabling signal input of the output stage (FINAL_STAGE) a replica of said enabling signal (OE) delayed by a period of said Internal clock signal (CK_IN).

2. The memory device of claim 1, wherein said output bus (PAD_EXT<3:0>) is a PCI bus and said state machine for controlling the data stream (OUTPUT_LPC) implements a Low Pin Count protocol.

3. The memory device of claim 1, wherein said enabling signal (OE) is generated after a period of said internal clock signal (CK_IN) starting from the instant at which the data to be output are provided to said state machine (OUTPUT_LPC).

4. The memory device of claim 1, wherein said delay circuit (FF) is a D type flip-flop synchronized by said internal clock signal (CK_IN).

5. The memory device of claim 1, wherein said delay circuit (FF) is included in the circuits of said state machine (OUTPUT_LPC).

6. The memory device of claim 1, wherein said standard memory core (FLASH_CORE) is a non volatile FLASH memory.

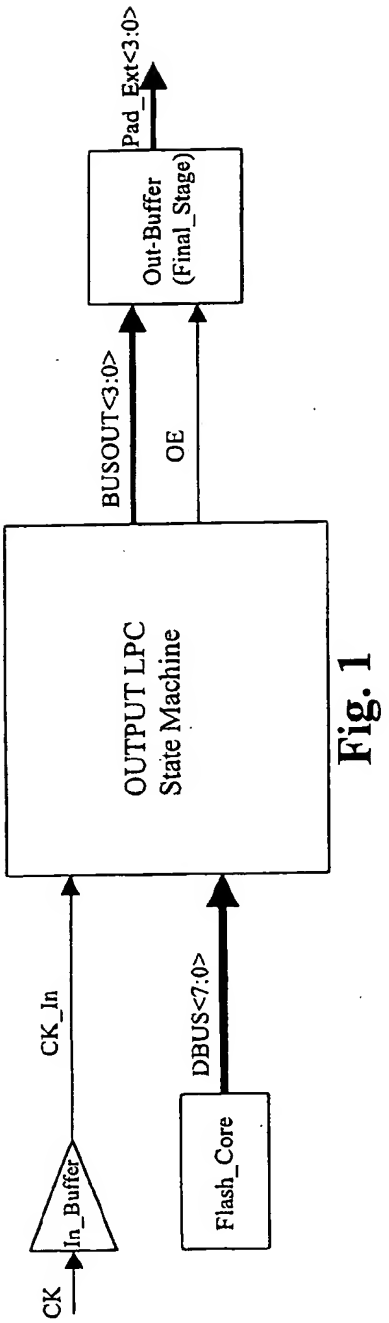
Pad_Ext<3:0>
Out-Buffer (Final_Stage)
BUSOUT<3:0>
OE
OUTPUT LPC State Machine
CK_In
DBUS<7:0>
In_Buffer
Flash_Core
CK

Fig. 1

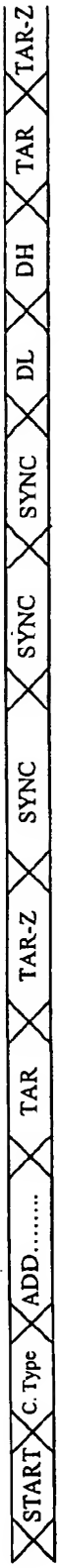
START
C. Type
ADD.....
TAR
TAR-Z
SYNC
SYNC
SYNC
DL
DH
TAR
TAR-Z

Fig. 2

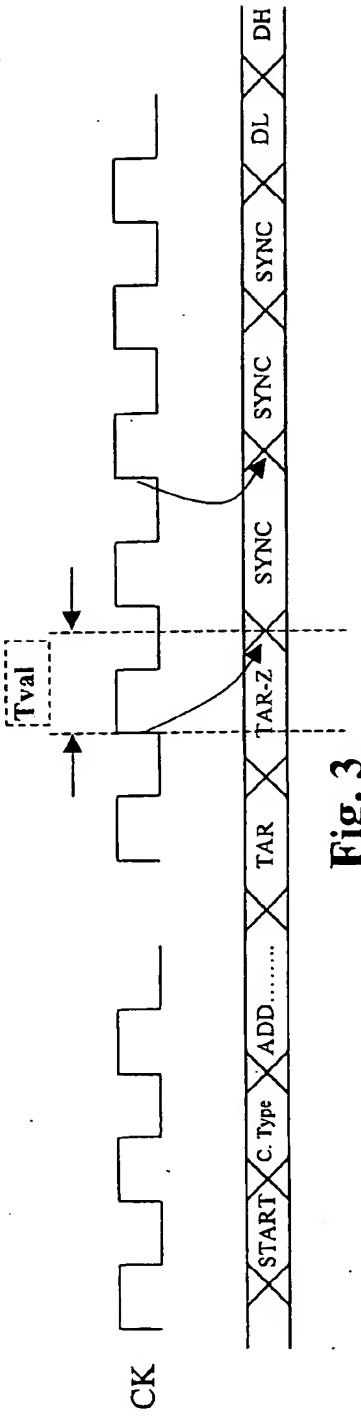
CK
START
C. Type
ADD.....
TAR
TAR-Z
SYNC
SYNC
SYNC
SYNC
DL
DH
Tval

Fig. 3

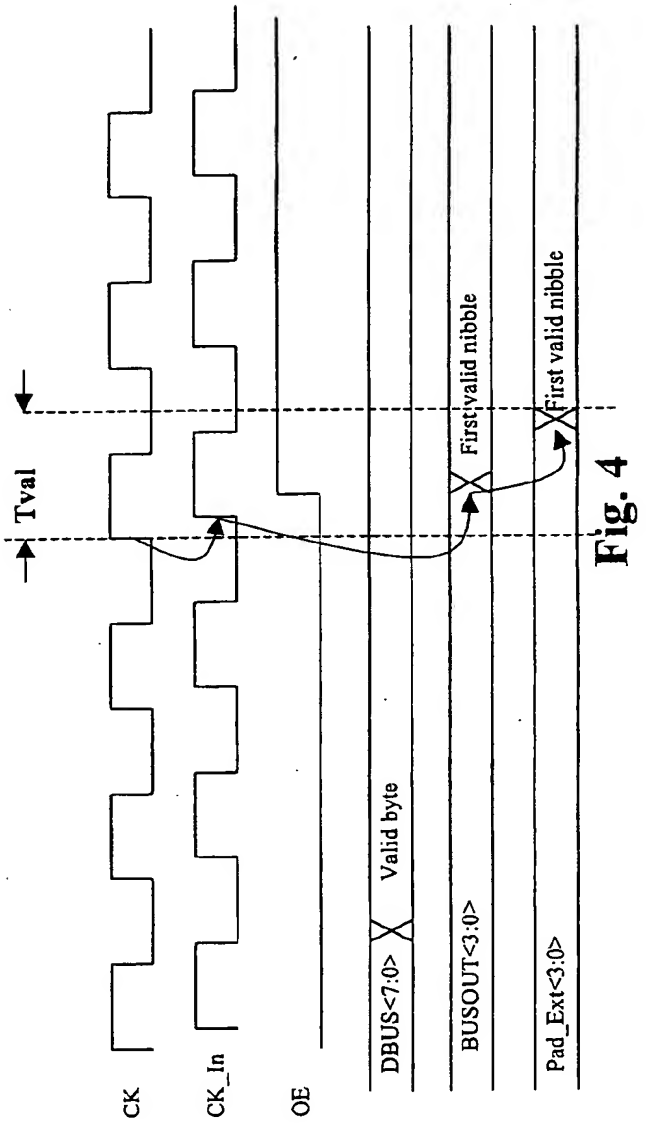
Tval
CK
CK_In
OE
DBUS<7:0>
Valid byte
BUSOUT<3:0>
First valid nibble
Pad_Ext<3:0>
First valid nibble

Fig. 4

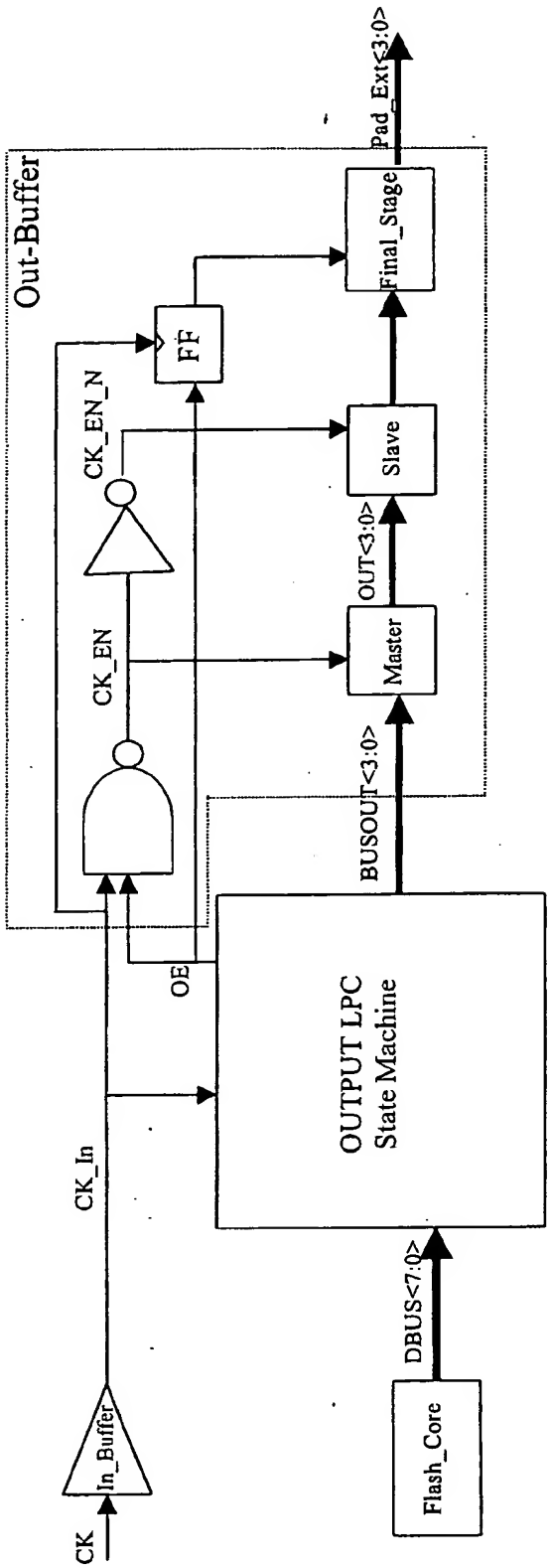
Out-Buffer
Pad_Ext<3:0>
Final_Stage
FF
CK_EN_N
Slave
OUT<3:0>
CK_EN
Master
BUSOUT<3:0>
OE
OUTPUT LPC
State Machine
CK_In
DBUS<7:0>
In_Buffer
Flash_Core
CK

Fig. 5

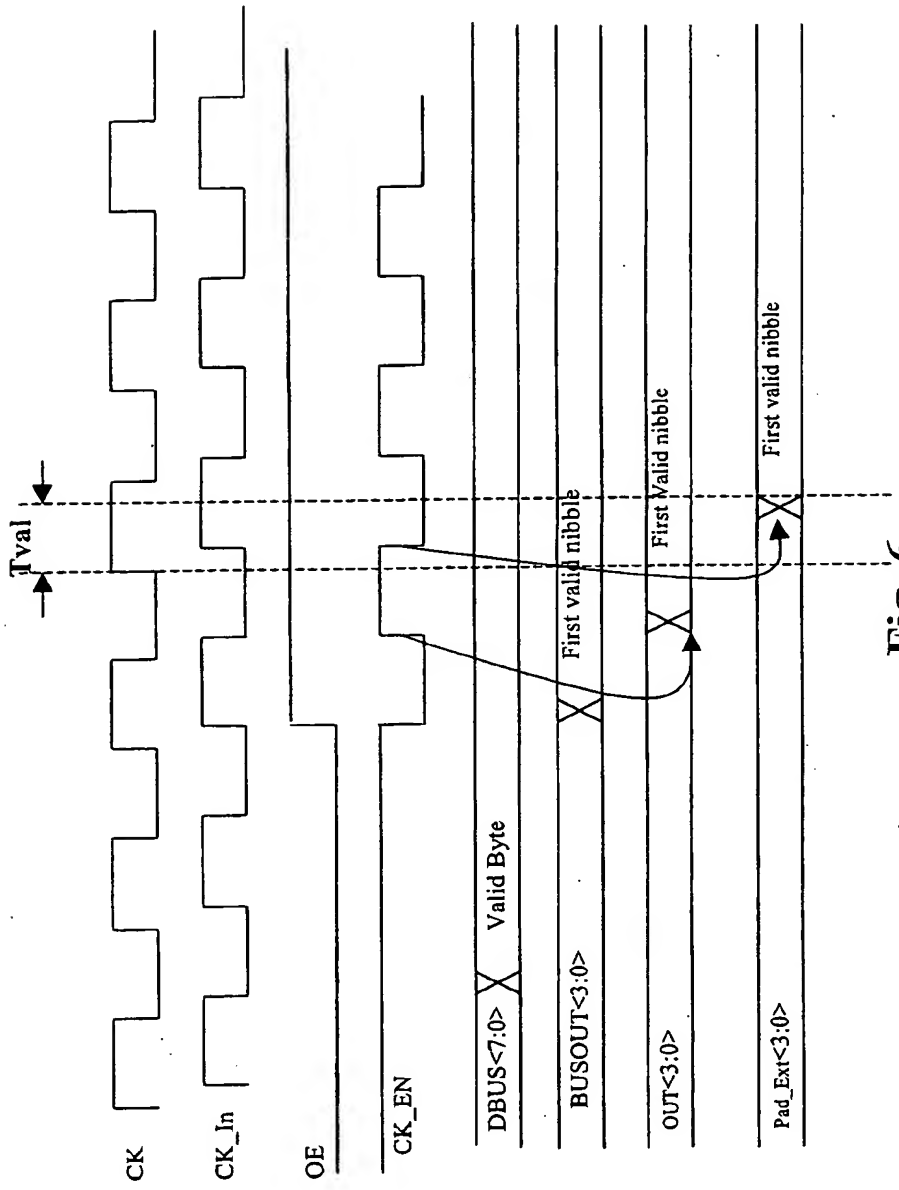
Tval
CK
CK_In
OE
CK_EN
DBUS<7:0>
Valid Byte
BUSOUT<3:0>
First valid nibble
OUT<3:0>
First Valid nibble
Pad_Ext<3:0>
First valid nibble

Fig. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 83 0782

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WO 99 15971 A (GAFKEN ANDREW H ;INTEL CORP (US); POISNER DAVID I (US); BENNETT JO) 1 April 1999 (1999-04-01) * figure 10 *	1,2,6	G11C16/26 G11C16/32 G11C7/10 G11C7/22 G06F13/42
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G11C
G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 May 2002	Vidal Verdu, J.

CATEGORY OF CITED DOCUMENTS

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 83 0782

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14-05-2002

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